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UNITED STATES PATENT APPLICATION

FOR

IMPROVING ELECTRO-STATIC DISCHARGE PROTECTION FOR HIGH FREQUENCY PORT ON AN INTEGRATED CIRCUIT

Inventor:

Jeffrey Johnson

Prepared by:

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP
12400 Wilshire Blvd., 7th Floor
Los Angeles, CA 90025-1026
(714) 557-3800

BACKGROUND

1. Field of the Invention

[001] This invention relates to electro-static discharge (ESD). In particular, the invention relates to ESD protection.

2. Description of Related Art

[002] Electro-static discharge (ESD) is a problem in integrated circuit (IC) technology. Typically, a Human Body Model (HBM) ESD event may be defined as an event where a current spike occurs that reaches approximately 90% of its maximum value in less than 10 nanoseconds (ns) and reduces to approximately 36% of its maximum value in less than 150 ns. An ESD event, if not properly handled, may destroy the internal circuitry of the integrated circuit where it occurs.

[003] Several ESD circuits have been designed to protect an IC from failure due to an ESD event. One circuit, known as a gate grounded N-channel Metal Oxide Semiconductor (GGNMOS) has an NMOS transistor with the gate being grounded at the output pin of the circuit. With the gate being grounded, the NMOS transistor behaves like a diode. Although this circuit is responsive to an ESD event, it increases the capacitive loading at the output and therefore degrades performance at high frequencies. Another type of circuit uses several transistors connected in series at the output pin at the circuit and connected to the gate of the driving transistor. This type of circuit, however, is slow in responding to an ESD event and can only provide a limited amount of protection.

[004] Therefore, there is a need to have an efficient technique to provide ESD protection at high frequencies.

BRIEF DESCRIPTION OF THE DRAWINGS

[005] The features and advantages of the present invention will become apparent from the following detailed description of the present invention in which:

[006] Figure 1 is a diagram illustrating a circuit package in which one embodiment of the invention can be practiced.

[007] Figure 2A is a diagram illustrating the circuit operating at normal high frequency mode.

[008] Figure 2B is a diagram illustrating the circuit operating at ESD event mode.

[009] Figure 3 is a flowchart illustrating a process to incorporate the inductor shown in Figure 1 in a package of the IC according to one embodiment of the invention.

DESCRIPTION

[0010] In the following description, for purposes of explanation, numerous details are set forth in order to provide a thorough understanding of the present invention. However, it will be apparent to one skilled in the art that these specific details are not required in order to practice the present invention. In other instances, well-known electrical structures and circuits are shown in block diagram form in order not to obscure the present invention.

[0011] It is noted that the invention may be described as a process which is usually depicted as a flowchart, a flow diagram, a structure diagram, or a block diagram. Although a flowchart may describe the operations as a sequential process, many of the operations can be performed in parallel or concurrently. In addition, the order of the operations may be re-arranged. A process is terminated when its operations are completed. A process may correspond to a method, a function, a procedure, a subroutine, a subprogram, etc. When a process corresponds to a function, its termination corresponds to a return of the function to the calling function or the main function.

[0012] Figure 1 is a diagram illustrating a circuit package or a circuit 100 in which one embodiment of the invention can be practiced. The circuit package 100 includes a high frequency integrated circuit 110 and a package substrate 115. The high frequency integrated circuit 110 includes a high frequency circuit 120, an ESD circuit 130, an ESD clamp circuit 140, bond pads 152, 154 and 156; and bond wires 172, 174 and 176. The package substrate 115 includes bond pads 162, 164 and 166, and an inductor 180.

[0013] The high frequency circuit 120 is a circuit operating at a high frequency. Typical operating frequency ranges at a gigahertz (GHz) level between 1 GHz to many GHz (e.g., 2.4 GHz). The high frequency circuit 120 includes a control circuit 122 and a drive circuit 124. The control circuit 122 generates a control signal to the drive circuit 124. The control circuit 122 may be a radio frequency (RF) circuit, a single-ended RF amplifier, a differential RF amplifier, or any digital or analog circuit that operates in this high frequency range.

[0014] The drive circuit 124 provides the driving output for the high frequency circuit 120. The drive circuit 124 is typically a transistor with a terminal connected to ground and an output terminal connected to provide a high frequency output.

[0015] The ESD circuit 130 is a circuit configured to provide ESD protection for the control circuit 122 and the drive circuit 124. The ESD circuit 130 may be a gate grounded NMOS transistor, a diode circuit, or any ESD protection circuit implemented through use of zener diodes, n-well resistors, polysilicon resistors, diffusion resistors, thin oxide field effect transistors (FETs), thick oxide FETs, low voltage trigger silicon controlled rectifiers (LVTSCRs), or a combination of any of these devices. The ESD circuit 130 may also be connected to the supply voltage instead of ground to respond to a possible ESD event.

[0016] The ESD clamp circuit 140 is connected between the power supply Vcc and the ground to clamp the voltage at a predetermined level to provide protection from a voltage surge or a high current spike when an ESD event occurs. An HBM ESD event may be defined as an event where a current spike occurs that reaches approximately 90% of its maximum value in less than 10 nanoseconds (ns) and reduces to approximately 36% of its maximum value in less than 150 ns. An ESD event may be negative or positive and the ESD circuit 130 is designed accordingly.

[0017] The control circuit 122, the drive circuit 124, the ESD circuit 130 and the ESD clamp circuit 140 are typically fabricated or manufactured to be on the same silicon die. During packaging, the silicon die is mounted on the package substrate. The package may be a ball grid array (BGA) or a flip-chip package. As is known by one skilled in the art, other packaging methods can be used. The bond pads 152, 154 and 156 are provided in the integrated circuit 110. The bond pad 152 provides connection terminal for one end the ESD clamp circuit 140 to the power supply Vcc. The other end of the ESD clamp circuit 140 is typically connected to ground. The bond pad 154 provides connection terminal to the output pin of the IC, or the output of the high frequency circuit 120. The bond pad 156 provides connection terminal to one end of the ESD circuit 130. The other end of the ESD circuit 130 is typically connected to ground. The bond pad 162 provides connection terminal directly to the power supply. A bond wire 172 is connected between the two bond pads 152 and 162. The bond pad 164 provides connection terminal for the high frequency output pin. The bond pad 164 is

also used to connect to one end of the inductor 180. The bond pad 166 provides connection terminal for the other end of the inductor 180. The bond pads 154 and 164 are connected via a bond wire 174. The bond pads 156 and 166 are connected via a bond wire 176.

[0018] The inductor 180 is connected in series or in line between the output of the high-frequency circuit 120 and the non-ground terminal of the ESD circuit 130 via bond wires 174 and 176. The inductor 180 may be fabricated using any PCB fabrication process. The inductor 180 has an inductance selected such that its impedance has a substantially high value at the operating frequency of the high frequency circuit and a substantially low value when the ESD event occurs.

[0019] Let Z, f, and L be the impedance (in Ohms, or Ω) of the inductor 180, the operating frequency of the high frequency circuit 120 (in Hertz), and the inductance of the inductor 180 (in Henry), respectively. The relationship among these values is given by the following equation:

$$Z = 2*\pi*f*L \qquad (1)$$

[0020] The inductance of the inductor 180 is selected such that at high frequencies, the inductor behaves like an open circuit and at the ESD event, or at low frequencies, it behaves like a short circuit. As an illustration, suppose L = 50 nanoHenry (nH). Then,

$$f = 2.4\ \text{GHz} = 2.4 \times 10^9\ \text{Hz} \rightarrow Z \cong 750\ \Omega \qquad (2)$$

$$f = 25\ \text{MHz} = 25 \times 10^6\ \text{Hz} \rightarrow Z \cong 7\ \Omega \qquad (3)$$

[0021] Table 1 below shows some values of the impedance for various values of the inductance and the frequency.

L(nH)	F	Z(Ω)	
50	10 MHz	3	Low frequency
	25 MHz	8	
	1 GHz	300	High frequency
	2.4 GHz	750	
	5 GHz	1500	
100	10 MHz	6	Low frequency
	25 MHz	16	
	1 GHZ	600	High frequency
	2.4 GHz	1500	
	5 GHz	3100	

Table 1

[0022] Figure 2A is a diagram illustrating the circuit operating at normal high frequency mode. In this mode, the high frequency circuit 120 operates normally at its operating frequency. The operating frequency may range from 1 GHz to many GHz. During normal mode, the ESD circuit 130 is not needed. Separating the ESD circuit 130 from the high frequency circuit 120 may be also beneficial in that the alternating current (AC) response of the high frequency circuit 120 may be enhanced or improved. As calculated above, at high frequencies, the impedance of the inductor 180 is approximately several hundred Ω. In addition, capacitive loading may also increase this impedance value even higher. This value is high enough so that the inductor 180 may behave like an open circuit, isolating the ESD circuit 130 from the high frequency output. This impedance is coupled in parallel with the load resistor at the output of the high frequency circuit 120. This load resistor may be approximately equal to 50 Ω. The equivalent resistance is therefore approximately 47Ω which is not far off the 50 Ω value. The resulting output impedance may attenuate the frequency response of the high frequency circuit 120 slightly, typically only a few percent. This slight attenuation does not reduce the circuit performance much, and therefore is acceptable when the high frequency circuit 120 operates at its normal operating frequency.

[0023] Figure 2B is a diagram illustrating the circuit operating at the ESD event mode. In this mode, an ESD event occurs. When this event occurs, the frequency of the current through the inductor 180 becomes low. At low frequencies, or when the an

ESD event occurs, the impedance of the inductor 180 is reduced to approximately less than 10 Ω. This value is low enough so that the inductor 180 behaves like a short circuit connecting the ESD circuit 130 to the high frequency output. In this way, the ESD circuit 130 may function or operate as a regular ESD circuit to protect the high-frequency circuit and the circuit package 100 from failure due to an ESD event.

[0024] For most practical purposes, the inductance of the inductor 180 may be selected to be approximately between 50 nH to 100nH. With this small value of inductance, the inductor 180 can be fabricated using standard Printed Circuit Board (PCB) technology to be part of the device in the package. The inductor 180 as such fabricated may occupy an area having dimensions of approximately 2 mm x 4mm. For a differential amplifier circuit having two high frequency circuits, two inductors may be used, one for each circuit.

[0025] Figure 3 is a flowchart illustrating a process 300 to incorporate the inductor shown in Figure 1 in a package of the IC according to one embodiment of the invention.

[0026] Upon START, the process 300 fabricates the high frequency circuit and the ESD circuit on the same silicon die (Block 310). After silicon die fabrication, the package substrate is manufactured with the inductor between bond pads 164 and 166 (Block 320). Next, the silicon die is mounted on the package substrate (Block 330). The packaging technology may be the ball grid array (BGA) or the flip-chip package. Then, the process 300 provides bond pads for the inductor, output of the high frequency circuit, and the non-ground terminal for the ESD circuit (Block 340). Next, the process 300 connects a bond wire between the high frequency pad and one end of the inductor and a bond wire between the ESD circuit pad and the bond pad of the other end of the inductor (Block 350). Then, the process 300 is terminated.

[0027] The present invention therefore provides an efficient means to enhance the ESD protection offered by the ESD circuit 130 (Figure 1) with negligible attenuation at the output. The ESD protection performance is improved by several times than with the ESD circuit used alone.

[0028] While this invention has been described with reference to illustrative embodiments, this description is not intended to be construed in a limiting sense. Various modifications of the illustrative embodiments, as well as other embodiments of the invention, which are apparent to persons skilled in the art to which the invention pertains are deemed to lie within the spirit and scope of the invention.